Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method ~~of~~ for high-speed header bypassing ~~of a programmable processing element~~, the method comprising:

receiving unencrypted data and a header associated with the unencrypted data;

under control of separation state machine logic, separating the header from the associated unencrypted data;

under control of first validation state machine logic, examining the header for format, number of bits and contents in order to validate the header;

~~examining data, the data including at least a header;~~

~~removing the header from the data;~~

encrypting the unencrypted data with a cryptographic algorithm to produce encrypted data ~~through a cryptographic component~~;

signaling second validation state machine logic from the first validation state machine logic when the header is determined to be valid, said signaling indicating a valid header is ready to transfer;

in response to said second validation state machine logic receiving said signaling from the first validation state machine, enabling transfer of the valid header to merge logic;

transferring the valid header to the merge logic around the cryptographic algorithm; and

~~rejoining~~ merging the ~~removed~~ valid header and the encrypted data with the merge logic~~; and~~

~~outputting the rejoined header and encrypted data~~.

2. (Currently Amended) The method of ~~bypassing a programmable processing element of~~ claim 1, and further comprising the second validation state machine logic signaling the first validation state machine logic to indicate readiness to accept the valid header ~~wherein the programmable processing element is at least one FPGA~~.

3-4. (Canceled)

5. (Currently Amended) The method of ~~bypassing a programmable processing element of~~ claim 1, wherein receiving comprises receiving the unencrypted data comprising ~~the data is~~ at least one of speech data~~,~~ and Ethernet data~~, or IC5232 data~~.

6-7. (Canceled)

8. (Currently Amended) The method of ~~bypassing a programmable processing element of~~ claim 1, wherein ~~the~~ one or more of said separating, examining, encrypting and merging is performed at a rate comparable to a data transfer rate of traffic carrying the unencrypted data ~~data occurs at traffic rates~~.

9 -13. (Canceled)

14. (Currently Amended) A system for high-speed header bypassing ~~programmable processing element, the element~~ comprising:

~~examination logic, the examination logic examining the input data, the input data including at least a header;~~

separation logic~~, the separation logic removing~~ that receives unencrypted data and a header associated with the unencrypted data and separates the header from the unencrypted data ~~examined data, the header being transferred outside an encryption component~~;

a separation state machine that controls the separation logic;

validation logic that examines the header for format, number of bits and contents in order to validate the header;

first validation state machine logic machine logic that controls the validation logic;

~~the~~ an encryption component that encrypts the unencrypted data with a cryptographic algorithm and produces encrypted data~~, wherein the encryption component includes a cryptographic element such that the data can be encrypted~~; ~~and~~

second validation state machine logic that is responsive to signaling from the first validation state machine logic indicating that the header is valid and is ready for transfer around said encryption component; and

merge logic~~, the merge logic rejoining~~ that merges the valid ~~removed~~ header and the encrypted data to be output;

wherein the second validation state machine logic enables transfer of the valid header to the merge logic in response to receiving said signaling from the first validation state machine logic.

15. (Currently Amended) The system ~~programmable processing element~~ of claim 14, wherein the second validation state machine logic signals the first validation state machine logic to indicate readiness to accept the valid header ~~programmable processing element is at least one FPGA~~.

16-18. (Canceled)

19. (Currently Amended) The system ~~programmable processing element~~ of claim 14, wherein one or more of the separation logic, validation logic, encryption component and merge logic operate at a rate comparable to a data transfer rate of traffic carrying the unencrypted data ~~the data further includes an internal Internet protocol header~~.

20-23. (Canceled)

24. (New) The method of claim 1, and further comprising the first validation state machine logic controlling a first door logic to open and permit transfer of the valid header; and the second validation state machine logic, in response to receiving said signaling from the first validation state machine logic, controlling a second door logic to open and permit the transfer of the valid header, supplied via said first door logic, to the merge logic.

25. (New) The system of claim 14, and further comprising first door logic coupled to the first validation state machine logic and second door logic coupled to the second validation state machine logic, the first door logic being connected to the second door logic, and wherein the first validation state machine logic controls the first door logic to open and permit transfer of the valid header, and the second validation state machine logic, in response to receiving said signaling from the first validation state machine logic, controls the second door logic to open and permit transfer of the valid header, supplied via said first door logic, to the merge logic.